REMARKS

Reconsideration of the above identified application in view of this Response is respectfully requested. This Response is in response to the Office Action dated May 16, 2007. By said Office Action, the Examiner stated the following detailed action items:

Item 1: claims 93 - 101 were withdrawn from consideration as being drawn to a non-elected invention, pursuant to 37 CFR 1.142(b).

Item 2: claims 18, 19, and 70, were withdrawn from consideration as being drawn to non-elected species, pursuant to 37 CFR 1.142(b).

Item 3: claims 1 - 17, 20 - 69, and 71 - 92, remain for examination.

Items 4 - 8: claims 1 - 2, 7 - 9, 11 - 14, 16, 17, 22, 25, 27 - 30, 35 - 36, 38 - 39, 41, and 44 - 49, were rejected under 35 U.S.C. 102(a) as being anticipated by Ein-Eli et al., "Silicon Texturing In Alkaline Media Conducted Under Extreme Negative Potentials", *Electrochem. & Solid State Letters*, 6(3): C47 - C50, 2003, as submitted on 2 November 2004 in Applicant's Information Disclosure Statement.

Items 9 - 14: claims 3 - 6, 10, 15, 23 - 24, 26, 31, 40, and 42 - 43, were rejected under 35 U.S.C. 103(a) as being unpatentable over Ein-Eli et al. in view of Starosvetsky et al. (US 6,521,118).

Items 15 - 17: claim 20 was rejected under 35 U.S.C. 103(a) as being unpatentable over Ein-Eli et al. in view of Sato (US 6,413,874).

Items 18 - 22: claims 21, 32 - 34, 37, and 50 - 52, were rejected under 35 U.S.C. 103(a) as being unpatentable over Ein-Eli et al..

Items 23 - 26: claims 53 - 69, and 71 - 92, were rejected under 35 U.S.C. 103(a) as being unpatentable over Ein-Eli et al. in view of Sato.

Items 27 - 31: claims 1 - 2, 7 - 9, 11 - 14, 16, 17, 22, 25, 27 - 30, 35 - 36, 38 - 39, 41, and 44 - 49, were rejected under 35 U.S.C. 103(a) as being unpatentable over Starosvetsky et al., "Environmentally Friendly, Fast Electrochemical Etching of Silicon", *Electrochemical Society Proceedings*, Proceedings Vol. 2002-14, pp 286 - 299 (Starosvetsky et al. '*Electro*), as submitted on 2 November 2004 in Applicant's Information Disclosure Statement.

Items 32 - 38: claims 3 - 6, 10, 15, 23 - 24, 26, 31 - 34, 40, and 42 - 43, were rejected under 35 U.S.C. 103(a) as being unpatentable over Starosvetsky et al. '*Electro* in view of Starosvetsky et al. (US 6,521,118).

Items 39 - 41: claim 20 was rejected under 35 U.S.C. 103(a) as being unpatentable over Starosvetsky et al. '*Electro* in view of Sato (US 6,413,874).

Items 42 - 46: claims 21, and 50 - 52, were rejected under 35 U.S.C. 103(a) as being unpatentable over Starosvetsky et al. '*Electro* in view of Vazsonyi et al., "Improved Anisotropic Etching Process for Industrial Texturing of silicon Solar Cells", *Solar Energy Materials & Solar Cells*, 57, 179 - 188, 1999, as submitted on 2 November 2004 in Applicant's Information disclosure Statement.

Items 47 - 50: claims 53 - 69, and 71 - 92, were rejected under 35 U.S.C. 103(a) as being unpatentable over Starosvetsky et al. '*Electro* in view of Sato.

By this Response, claims 1 - 17, 20 - 69, and 71 - 92, remain as originally filed.

The Examiner is respectfully made aware that the US Patent Application Publication, to Ein-Eli, et al., having Pub. No.: US 2005/0148198 A1, and Pub. Date: July 07, 2005, of the present U.S. Pat. Appl. No. 10/750,969, was used for preparing the present Response. Accordingly, Applicant's references to page and paragraph numbers correspond to those of the just stated publication of the present patent application document.

Briefly, the present invention relates to texturing a semiconductor material using negative potential dissolution (NPD), by applying 'atypically' highly negative (cathodic) potentials during conditions of wet etching. Semiconductor material is subjected to wet etching conditions, negative biasing at more negative than -60 V, and, specifically controlled and directed illumination by optically processed non-ambient light, *unexpectedly* resulting in significant increase in values of cathodic current density, and, rate and extent of texturing, of the semiconductor material as a function of time. As cut unpolished semiconductor material is subjected to wet etching conditions and negative biasing, during non-specifically controlled and directed illumination by unprocessed ambient light. Illumination of the as cut unpolished semiconductor material is not needed for increasing values of cathodic current density, and, rate and extent of the texturing. Particularly applicable to manufacturing solar cells from semiconductor materials.

Claim Rejections - 35 U.S.C. 102

In Examiner Items 4 - 8, the Examiner rejected claims 1 - 2, 7 - 9, 11 - 14, 16, 17, 22, 25, 27 - 30, 35 - 36, 38 - 39, 41, and 44 - 49, under 35 U.S.C. 102(a), as being anticipated by Ein-Eli et al., "Silicon Texturing In Alkaline Media Conducted Under Extreme Negative Potentials", *Electrochem. & Solid State Letters*, 6(3): C47 - C50, 2003, as submitted on 2 November 2004 in Applicant's Information Disclosure Statement".

The Examiner's claim rejections are respectfully traversed.

First, the Applicant respectfully points out to the Examiner that the cover page of the Applicant's Information Disclosure Statement, dated October 28, 2004, and submitted on November 02, 2004, includes the statements: "Enclosed is a PTO Form 1449 which lists citations which may be material to the patentability and examination of the above identified application", and "This Information Disclosure Statement under 37 CFR 1.56 is not to be construed as a representation that a search has been made, that additional matter which is material to the examination of this application does not exist, or that any one or more of these citations constitutes prior art". Moreover, in accordance with MPEP 2129 (IV), "Mere listing of a reference in an information disclosure statement is not taken as admission that the reference is prior art against the claims".

Second, the Applicant respectfully points out to the Examiner that the Ein-Eli et al. publication was authored (solely) by the same Applicant of the present invention, and more particularly, by Yair Ein-Eli and David Starosvetsky, being two of the same inventors of the present invention disclosed in the present patent application. Moreover, the Applicant declares that the Applicant's Ein-Eli et al. publication describes the same invention invented by the same Applicant and by the same inventors of the present invention disclosed in the present patent application. The present invention disclosed in the present patent application is derived from Applicant's own work described in the Ein-Eli et al. publication. There is no dispute or inconsistency as to inventorship of the invention described in the Applicant's Ein-Eli et al. publication and the same invention disclosed in the same Applicant's present patent application.

The Applicant believes that the preceding discussion completely overcomes the Examiner's claim rejections under 35 U.S.C. 102(a), as stated in Examiner Items 4 - 8.

In view of the preceding discussion regarding overcoming the Examiner's claim rejections under 35 U.S.C. 102(a), the Applicant respectfully points out to the Examiner

that the Applicant's present patent application was filed on Jan. 05, 2004, whereas the Applicant's Ein-Eli et al. publication was first made public (that is, first made "Available electronically January 14, 2003", as clearly stated immediately beneath the abstract of the Ein-Eli et al. publication) on January 14, 2003. Thus, clearly, the present patent application was filed within the allowable one (1) year grace period (which terminated on January 14, 2004) of public disclosure of the present invention. Therefore, the Applicant's Ein-Eli et al. publication is inapplicable as being classified and cited as prior art under 35 U.S.C. 102(b) against the claims of the present application.

The preceding discussion precludes the Examiner from citing the Ein-Eli et al. publication in a claim rejection under 35 U.S.C. 102(b).

Claim Rejections - 35 U.S.C. 103

In Examiner Items 9 - 14, the Examiner rejected claims 3 - 6, 10, 15, 23 - 24, 26, 31, 40, and 42 - 43, under 35 U.S.C. 103(a), as being unpatentable over Ein-Eli et al. in view of Starosvetsky et al. (US 6,521,118).

The Examiner's claim rejections are respectfully traversed.

In view of the preceding discussion regarding overcoming the Examiner's claim rejections under 35 U.S.C. 102(a), and precluding citation of the Applicant's Ein-Eli et al. publication in a claim rejection under 35 U.S.C. 102(b), the Applicant respectfully points out to the Examiner that, since the criteria for classifying and citing a publication as prior art under 35 U.S.C. 103 are the same as those for classifying a publication as prior art under 35 U.S.C. 102, therefore, the Applicant's Ein-Eli et al. publication is inapplicable as being classified and cited as prior art under 35 U.S.C. 103(a) against the claims of the present application. Moreover, in the present Examiner's 35 U.S.C. 103(a) claim rejections of Examiner Items 9 - 14, the Applicant's Ein-Eli et al. publication is indicated as the *primary* (prior art) reference. However, since the Applicant's Ein-Eli et al. publication is inapplicable as being classified and cited as prior art under 35 U.S.C. 103(a) against the claims of the present application, therefore, the present Examiner's 35 U.S.C. 103(a) claim rejections are deemed moot.

The Applicant believes that the preceding discussion completely overcomes the Examiner's claim rejections based on grounds of 35 U.S.C. 103(a), as stated in Examiner Items 9 - 14.

In Examiner Items 15 - 17, the Examiner rejected claim 20 under 35 U.S.C. 103(a) as being unpatentable over Ein-Eli et al. in view of Sato (US 6,413,874).

In Examiner Items 18 - 22, the Examiner rejected claims 21, 32 - 34, 37, and 50 - 52, under 35 U.S.C. 103(a) as being unpatentable over Ein-Eli et al..

In Examiner Items 23 - 26, the Examiner rejected claims 53 - 69, and 71 - 92, under 35 U.S.C. 103(a) as being unpatentable over Ein-Eli et al. in view of Sato.

The Examiner's claim rejections are respectfully traversed.

The Applicant contends that the above discussion for overcoming the Examiner's claim rejections under 35 U.S.C. 103(a) regarding Examiner Items 9 - 14, is similarly applicable for overcoming the Examiner's claim rejections under 35 U.S.C. 103(a) regarding Examiner Items 15 - 17, 18 - 22, and 23 - 26.

In Examiner Items 27 - 31, the Examiner rejected claims 1 - 2, 7 - 9, 11 - 14, 16, 17, 22, 25, 27 - 30, 35 - 36, 38 - 39, 41, and 44 - 49, under 35 U.S.C. 103(a) as being unpatentable over Starosvetsky et al. '*Electro*.

The Examiner's claim rejections are respectfully traversed.

In Examiner Item 28, in regard to (independent) claim 1, among other (dependent) claims, the Examiner stated that: ". . . Starosvetsky et al. '*Electro*. discloses a method for texturing a semiconductor material, . . . under the claimed process variable conditions . . . (pp. 287 - 288 and 294). Starosvetsky et al. '*Electro*. does not specifically disclose value of cathodic current density of the semiconductor material is significantly higher at end of illumination time period than at beginning of time period *(as recited in step (c) of claim 1)*. However, since Starosvetsky et al. '*Electro*. has the same active method steps (i.e., applying a negative bias for a period of time), thus claimed current response would be inherent to Starosvetsky et al. '*Electro's* method, thus meeting the claimed invention".

Additionally, in Examiner Item 29, the Examiner stated that: "However, Starosvetsky et al. '*Electro*. does not specifically disclose negative bias to a potential more than 60 relative to standard reference electrode. Starosvetsky et al. '*Electro*. shows that - 60 V is used and thus is very close to - 60.01 V (a voltage greater than - 60V); there is no patentable distinction between values that are so close unless criticality or unexpected results can be shown".

The Applicant firmly contends even though Starosvetsky et al. '*Electro*. has the same (general) active method steps (i.e., applying a negative bias and illuminating for a

period of time), that by performing the Starosvetsky et al. '*Electro.* method in accordance with step (b) of claim 1, that is, "negatively biasing the semiconductor material to a potential more negative than minus sixty volts relative to a standard reference electrode", the claimed *(time dependent)* current response, that is, "the value of cathodic current density of the semiconductor material is significantly higher at the end of the illumination time period than at the beginning of the illumination time period", would NOT be inherent to Starosvetsky et al. '*Electro's* method, thus NOT meeting the claimed invention.

Moreover, the Applicant firmly contends that there clearly and unambiguously is patentable distinction, based on criticality and unexpected results, between the value of the negative potential recited in step (b) of claim 1, that is, "more negative than minus sixty volts relative to a standard reference electrode", of the present invention, and the values of negative potentials taught by Starosvetsky et al. '*Electro.*, either singly or in combination with other prior art teachings.

In strong contrast to the illustrative description (text and figures) of the present invention, which fully supports the entire recitation of claim 1, particularly, recitations of steps (b) and (c), there is throughout the entire Starosvetsky et al. '*Electro.* publication (pages 286 - 299), absolutely no explicit (literal or figurative) or implicit (suggestive) teaching regarding the patentably important parameter or affect of time dependency, period of time, or time duration, upon the current response (i.e., etch (etching) rate, or current (cathodic current density)) resulting from performing the silicon etching experiments at negative potentials, either under illumination, or in the dark.

Throughout the entire Starosvetsky et al. '*Electro.* publication there are only two (briefly passing) mentions of time. The first mention of time is found therein on the top of page 294, in the Results section, in the sub-section entitled: '*Effect of Applied negative Potential on Silicon Topography*', wherein it is stated: "These images *(i.e., shown in Fig. 5)* characterize the topography of the silicon samples treated in KOH at 60 °C for one hour in dark at the OCP, 10, 20, and -40 V", and further therein, wherein it is stated: "Similar surface examination was also conducted for p-Si etched at cathodically applied voltages under illumination". The second, and only other, (briefly passing) mention of time is found on the middle of page 296, also in the Results section, in the sub-section entitled: '*SIMS examination*', wherein it is stated: "Depth compositions profiles of sodium and hydrogen in n-Si after one hour of polarization in 24 % sodium hydroxide (NaOH) at - 40 V and in an as-received sample are shown in Fig. 7".

Moreover, in Starosvetsky et al. '*Electro*., on page 287, in the Introduction section, and on page 290, the authors made reference to their own previous (related) work on the same subject. Namely, reference number 12, which on page 299 therein, is listed as: "D. Starosvetsky, M. Kovler, Y. Yahalom, and Y. Nemirovsky, Israel Patent Application # 122937/3 (14 January 1998), PCT pending", which is a prior art document corresponding to Starosvetsky et al. (US 6,521,118). The authors of the Starosvetsky et al. '*Electro*. publication [three of which are inventors of the invention disclosed in Starosvetsky et al. (US 6,521,118)], performed the cathodic biased and illuminated or darkened silicon wet etching experiments in the same manner and using the same equipment as they performed the cathodic biased and illuminated or darkened silicon wet etching experiments described in Starosvetsky et al. (US 6,521,118). Namely, etch (etching) rate, or current (cathodic current density)) resulting from performing the silicon etching experiments at negative potentials, either under illumination, or in the dark, was measured as a function of time, during which the etch (etching) rate, or current (cathodic current density)) always attained a constant value which remained constant during the 'entire' time period or time duration of the illumination, or in the dark, measurements.

Accordingly, in Starosvetsky et al. '*Electro*., in the Results section, in the sub-section entitled: '*Silicon Etching at negative potentials*', on page 291, in Figure 3, and on page 292, in Figure 4, the experimental results of etch (etching) rate, or current (cathodic current density)) plotted as a function of potential, V(SCE), correspond to values which are constant and time independent for the conditions studied. Therein, there is absolutely no explicit (literal or figurative) or implicit (suggestive) teaching regarding the patentably important parameter or affect of time dependency, period of time, or time duration, upon the current response (i.e., etch (etching) rate, or current (cathodic current density)) resulting from performing the silicon etching experiments at negative potentials, either under illumination, or in the dark.

For the purpose of additionally clearly showing patentable distinction between the method of the present invention, as claimed in independent claim 1 (and dependent claims thereof), and the method described in the Starosvetsky et al. '*Electro*. publication, either singly or in combination with the invention described in Starosvetsky et al. (US 6,521,118), or for that matter, in combination with any number of other prior art teachings, the Applicant respectfully points out to the Examiner that the preceding described (prior art) teachings of cathodic biased and illuminated or darkened silicon wet etching experiments are clearly confirmed in the specification of the present application.

Moreover, the inventive features recited in claim 1, with particular attention and focus on the recitations of steps (b) and (c), are clearly exemplified, described in relation to, and distinguished from, the preceding described (prior art) teachings of cathodic biased and illuminated or darkened silicon wet etching experiments.

Specifically, for example, in the Applicant's present patent application, on page 23, paragraphs [0193] - [0204], along with reference to FIGS. 2 and 3, in the Examples section, in Example 1, regarding 'Texturing Polished <100> p-type Silicon Using Negative Potential Dissolution (NPD)'. Therein, in paragraphs [0203] - [0204], in the 'Results and Discussion' sub-section it is stated:

[0203] "Two characteristic negative potential regions were observed, each characterized by a different profile of values of cathodic current density, measured during sample illumination. As shown in FIG. 2, down to -60 V, the value of cathodic current density remained practically independent of the applied potential during an exposure time of about 5000 seconds. At negative potentials more negative than -60 V, the value of cathodic current density gradually increased. The value of cathodic current density measured from the silicon sample, during exposure at a negative potential of -80 V, slowly increased from 0.48 to 0.68 A/cm^2. However, another increase in the measured value of cathodic current density was detected when the applied negative potential was shifted to more negative values. FIG. 2 shows that the value of cathodic current density measured from the silicon electrode during NPD at -100 V increased faster, from -0.48 to 1 A/cm^2 during a time period of 3300 sec, than the value of cathodic current density measured at the negative potential of -80 V".

[0204] "The values of the initial cathodic current density measured immediately after illuminating the silicon electrodes ("Initial" curve), and at the end-point of each experiment ("Final" curve) are summarized in FIG. 3. The difference between the initial and the final values of cathodic current density was detected only in the potential range more negative than -60 V. Once a shift in the applied potential in the negative direction is maintained, this difference dramatically increased. At potentials less negative than -60 V, the initial and final values of cathodic current density practically coincided".

In addition to the preceding discussion, which includes clear and unambiguous discussion of experimental evidence showing criticality and unexpected results, for distinguishing the inventive features recited in claim 1, with particular attention and focus on the recitations of steps (b) and (c), as illustratively described, and exemplified, in the Applicant's present application, from the teachings of Starosvetsky et al. '*Electro*, either

singly or in combination with other prior art teachings, the Applicant respectfully directs the Examiner's attention to the Applicant's present application, in the 'Field And Background Of The Invention' section, on page 2, paragraphs [0009] - [0011], wherein it is stated:

[0009] "Nevertheless, the above disclosures by the same inventors of the present invention are somewhat limited in the following several respects".

[0010] "First, therein is teaching of applying the negative potential dissolution (NPD) technique combined with illumination for negative potentials down to only minus fifty volts relative to a standard calomel electrode (SCE). As long as a semiconductor material, such as silicon, remains intact and active, as opposed to becoming inactivated and/or deactivated, during the negative biasing combined with illumination procedure, there is need for investigating and establishing the applicable conditions and controlling operating parameters, and the affects and characteristics, of subjecting a semiconductor material to negative potentials more negative than minus fifty volts. Applicable conditions and controlling operating parameters, and affects and characteristics, of subjecting a semiconductor material to negative potentials down to minus fifty volts are not obviously extendable to subjecting the semiconductor material to negative potentials more negative than minus fifty volts".

[0011] "Moreover, for example, in the disclosure of U.S. Patent No. 6,521,118, in particular, as seen in Fig. 2 therein, it was consistently observed that immediately following initiation of illuminating the negatively biased silicon wafer exposed to the NaOH etching solution, the values of cathodic current density, and therefore, rate and extent of texturing of the surface, suddenly and significantly increased, nearly in a step-like manner, but, the values remained essentially constant thereafter as a function of time. Therein, there is no teaching about searching for and establishing conditions and controlling operating parameters which may give rise to increasing values of cathodic current density, and therefore, increasing rate and extent of texturing of the surface, as a function of time during the negative biasing combined with illumination procedure".

In view of the preceding discussion, including clear and unambiguous discussion of experimental evidence showing criticality and unexpected results, the Applicant strongly believes and firmly contends that the inventive features recited in claim 1, with particular attention and focus on the recitations of steps (b) and (c), as illustratively described, and

exemplified, in the Applicant's present application, are clearly NOT inherent to, or obvious over, Starosvetsky et al. '*Electro's* method, either singly or in combination with other prior art teachings.

The Applicant believes that the preceding discussion completely overcomes the Examiner's rejection of (independent) claim 1 under 35 U.S.C. 103(a), as stated in Examiner Items 27 - 29.

Thus, in view of the preceding discussion regarding overcoming the Examiner's rejection of (independent) claim 1 under 35 U.S.C. 103(a), and in view of the above discussion regarding overcoming the Examiner's rejection of (independent) claim 1 under 35 U.S.C. 102(a), as stated in Examiner Items 4 - 6, the Applicant believes that (independent) claim 1, and therefore, dependent claims 2 - 17, and 20 - 52, therefrom, are in allowable condition and such action is respectfully requested.

In Examiner Items 47 - 50, the Examiner rejected claims 53 - 69, and 71 - 92, under 35 U.S.C. 103(a) as being unpatentable over Starosvetsky et al. '*Electro* in view of Sato.

The Examiner's claim rejections are respectfully traversed.

In Examiner Item 48, the Examiner stated that: "Starosvetsky et al. '*Electro*. in view of Sato discloses the claimed method as stated above in paragraphs *(Examiner Items)* 28 - 29 and 40 - 41. Furthermore, Starosvetsky et al. '*Electro*. discloses a method wherein the illumination is less than 0.01 watts per cm^2 (Figure 4; p. 292). Starosvetsky et al. '*Electro*. does not specifically disclose the value of current density as a function of time with the claimed initial rise to a maximum and subsequent decreases to a series of values each being significantly less than the maximum value *(as recited in step (b) of each claim 53 and 92)*. However, since Starosvetsky et al. '*Electro*. in view of Sato has the same active method steps (i.e., applying a negative bias for a period of time), thus claimed current response would be inherent to Starosvetsky et al. '*Electro* in view of Sato's method, thus meeting the claimed invention".

Additionally, in Examiner Item 49, in regard to (independent) claim 53, among other (dependent) claims, the Examiner referred back to previously presented Examiner paragraphs (*Items*), regarding Examiner's claim rejections of (independent) claim 1 and dependent claims therefrom.

Additionally, in Examiner Item 50, in regard to (independent) claim 92, the Examiner referred back to previously presented Examiner paragraphs (*Items*), regarding Examiner's claim rejections of (independent) claim 1 and dependent claims therefrom.

Similar to Applicant's hereinabove response to Examiner's claim rejection of (independent) claim 1, the Applicant firmly contends even though Starosvetsky et al. '*Electro*. in view of Sato has the same (general) active method steps (i.e., applying a negative bias for a period of time), that by performing the Starosvetsky et al. '*Electro*. method in view of Sato's method, in accordance with step (b) of claim 53 or of claim 92, that is, "negatively biasing the as cut unpolished semiconductor material to a negative potential of at least minus one volt relative to a standard reference electrode for a period of time, during which the as cut unpolished semiconductor material is illuminated by light at an intensity of less than 0.01 watts per cm^2", or "negatively biasing the as cut unpolished semiconductor material to a negative potential of at least minus one volt relative to a standard reference electrode for a period of time", respectively, the claimed *(time dependent)* current response, that is, "the value of cathodic current density of the as cut unpolished semiconductor material as a function of time during the time period initially increases to a maximum value, then decreases to a series of values each being significantly less than the maximum value", would NOT be inherent to Starosvetsky et al. '*Electro* in view of Sato's method, thus NOT meeting the claimed invention.

Moreover, the Applicant firmly contends that there clearly and unambiguously is patentable distinction, based on criticality and unexpected results, of the time dependent current response (i.e., etch (etching) rate, or current (cathodic current density)) recited in step (b) of claims 53 and 92, that is, "the value of cathodic current density of the as cut unpolished semiconductor material as a function of time during the time period initially increases to a maximum value, then decreases to a series of values each being significantly less than the maximum value", of the present invention, and the values of current response (i.e., etch (etching) rate, or current (cathodic current density)) taught by Starosvetsky et al. '*Electro*. in view of Sato, or, additionally in view of other prior art teachings.

As stated hereinabove, in Applicant's response to Examiner's claim rejection of (independent) claim 1, in strong contrast to the illustrative description (text and figures) of the present invention, which fully supports the entire recitations of claim 53 and 92, particularly, recitations of steps (b) and (c), there is throughout the entire Starosvetsky et al. '*Electro*. publication (pages 286 - 299), absolutely no explicit (literal or figurative) or implicit (suggestive) teaching regarding the patentably important parameter or affect of time dependency, period of time, or time duration, upon the current response (i.e., etch (etching) rate, or current (cathodic current density)) resulting from performing the silicon etching experiments at negative potentials, either under illumination, or in the dark.

Similarly, as stated hereinabove, in Applicant's response to Examiner's claim rejection of (independent) claim 1, in Starosvetsky et al. '*Electro.*, in the Results section, in the sub-section entitled: '*Silicon Etching at negative potentials*', on page 291, in Figure 3, and on page 292, in Figure 4, the experimental results of etch (etching) rate, or current (cathodic current density)) plotted as a function of potential, V(SCE), correspond to values which are constant and time independent for the conditions studied. Therein, there is absolutely no explicit (literal or figurative) or implicit (suggestive) teaching regarding the patentably important parameter or affect of time dependency, period of time, or time duration, upon the current response (i.e., etch (etching) rate, or current (cathodic current density)) resulting from performing the silicon etching experiments at negative potentials, either under illumination, or in the dark.

For the purpose of additionally clearly showing patentable distinction between the method of the present invention, as claimed in independent claims 53 and 92 (and dependent claims thereof), and the method described in the Starosvetsky et al. '*Electro.* publication in view of Sato, or additionally in view of the invention described in Starosvetsky et al. (US 6,521,118), or for that matter, additionally in view of any number of other prior art teachings, the Applicant respectfully points out to the Examiner that the above described (prior art) teachings of cathodic biased illuminated or darkened silicon wet etching experiments are clearly confirmed in the specification of the present application. Moreover, the inventive features recited in claims 53 and 92, with particular attention and focus on the recitations of steps (b) and (c), are clearly exemplified, described in relation to, and distinguished from, the preceding described (prior art) teachings of cathodic biased and illuminated or darkened silicon wet etching experiments.

Specifically, for example, in the Applicant's present patent application, on page 25, paragraphs [0215] - [0222], and [0227] - [0228], along with reference to FIGS. 5, 6, and 9, in the Examples section, in Example 2, regarding 'Texturing 'As Cut Unpolished <110> and <111> p-type Silicon Using Negative Potential Dissolution (NPD)'. Therein, in paragraphs [0221] - [0222], and [0227] - [0228], in the 'Results and Discussion' sub-section it is stated:

[0221] "As shown in FIG. 5, the cathodic current density reached values of -0.019 and about -0.25 A/cm^2, at -10 V and -20 V, respectively, within a short time following initiation of the negative biasing. Further exposure to the cathodic bias did not practically change the value of cathodic current density. At a cathodic voltage of -40 V, the shape of the current-time curve markedly changed, becoming a type of 'U' shape: the

value of cathodic current density soared to a maximum value immediately following initiation of the negative biasing, slowly decreased with time and reaching a minimum, followed by a gradual increase during further application of the negative biasing. The shift in the applied potential from -40 V to more negative values resulted in sufficient increase in the value of cathodic current density, and marked increase in the rate of the texturing stages. As seen in FIG. 5, the decrease in value of cathodic current density to the minimum and its second increase, occurred more rapidly once the applied potential was shifted to more highly negative values".

[0222] "It was established that the 'U' shape current-time profile obtained with the as cut unpolished <110> p-type Si is characteristic for all the studied orientations of as cut unpolished p-type Si at potentials more negative than -20V. FIG. 6 is an empirically determined graphical plot of cathodic current density (A/cm^2) measured as a function of time (sec), of the as cut unpolished <110> p-type silicon wafer, and the as cut unpolished <111> p-type silicon wafer, during separately exposing each to a potassium hydroxide (KOH) etching solution, 24 wt %, at 20 °C, negative biasing at a negative (cathodic) potential of -40 V, and -45 V, respectively, relative to a standard calomel reference electrode (SCE), during dark conditions of non-specifically controlled and directed illumination by light, in particular, in the form of unprocessed surrounding or background ambient light having an intensity of less than 0.01 watts per cm^2 incident upon the negatively biased as cut unpolished silicon surface. As is seen, all the curves obtained with the as cut unpolished p-type Si electrodes with different orientation had the 'U' shape profile. The major differences between the profiles presented in FIG. 6 were the measured values of cathodic current density and the duration of the texturing".

[0227] "FIG. 9 is a graphical plot of cathodic current density (A/cm^2) as a function of time (sec), representing an exemplary proposed model graphically illustrating the multi-phenomenological behavior, including the 'U' shape profile, of the value of cathodic current density of an as cut unpolished semiconductor material as a function of time, during the negative biasing time period, during dark conditions. The initial increase in the value of cathodic current density observed in the first seconds is most probably due to the existence of numerous surface defects and/or defect zones in the as cut unpolished silicon samples. The following decrease in the value of cathodic current density is due to two parallel surface processes simultaneously taking place: (i) removal of surface defects and/or defect zones, and (ii) initial surface texturing. The extensive plateau at almost constant low values of cathodic current density reflects texturing of the silicon surface,

while the rapid increase in the value of cathodic current density is most likely due to surface area increase caused by an extensively over-textured surface".

[0228] "Clearly, the rate and extent of texturing of the silicon surfaces, and therefore, the type of textured silicon surfaces formed therefrom, are controllable and significantly influenced by the several primary operating conditions and parameters of the negative potential dissolution (NPD) technique, such as type of the semiconductor material; type, concentration, temperature, and flow rate, of the etching solution; and, magnitude and duration of the negative biasing".

In addition to the preceding discussion, which includes clear and unambiguous discussion of experimental evidence showing criticality and unexpected results, for distinguishing the inventive features recited in claims 53 and 92, with particular attention and focus on the recitations of steps (b) and (c), as illustratively described, and exemplified, in the Applicant's present application, from the teachings of Starosvetsky et al. '*Electro* in view of Sato, or additionally in view of other prior art teachings, the Applicant respectfully directs the Examiner's attention to the Applicant's present application, in the 'Field And Background Of The Invention' section, on page 2, paragraph [0012], wherein it is stated:

[0012] "Second, therein is teaching of applying the negative potential dissolution (NPD) technique combined with illumination to only polished semiconductor materials, in particular, polished p-type silicon or polished n-type silicon waters. In various fields, particularly in the field of manufacturing solar cells or photovoltaic panels, 'as cut unpolished' semiconductor materials are subjected to surface texturing processes for the objective of decreasing reflectance of incident sunlight away from the semiconductor material surfaces. Accordingly, there is need for investigating and establishing the applicable conditions and controlling operating parameters, and affects and characteristics, of subjecting an 'as cut unpolished' semiconductor material to the negative potential dissolution (NPD) technique, either combined with illumination or performed without illumination of the negatively biased as cut semiconductor material exposed to the etching solution. Since polishing an 'as cut unpolished' semiconductor material tends to significantly change the surface morphology and topology of the original as cut unpolished semiconductor material, applicable conditions and controlling operating parameters, and affects and characteristics, of subjecting a polished semiconductor material to the negative potential dissolution (NPD) technique, are not obviously extendable to subjecting an as cut

unpolished semiconductor material to the same negative potential dissolution (NPD) technique".

In view of the preceding discussion, including clear and unambiguous discussion of experimental evidence showing criticality and unexpected results, the Applicant strongly believes and firmly contends that the inventive features recited in claims 53 and 92, with particular attention and focus on the recitations of steps (b) and (c), as illustratively described, and exemplified, in the Applicant's present application, are clearly NOT inherent to, or obvious over, Starosvetsky et al. '*Electro* in view of Sato's method, or additionally in view of other prior art teachings.

The Applicant believes that the preceding discussion completely overcomes the Examiner's rejection of (independent) claims 53 and 92 under 35 U.S.C. 103(a), as stated in Examiner Items 47 - 50.

Thus, in view of the preceding discussion regarding overcoming the Examiner's rejection of (independent) claims 53 and 92 under 35 U.S.C. 103(a), and in view of the above discussion regarding overcoming the Examiner's rejection of (independent) claims 53 and 92 under 35 U.S.C. 103(a), as stated in Examiner Items 23 - 26, the Applicant believes that (independent) claim 53, and therefore, dependent claims 54 - 69, and 71 - 91 therefrom, and that (independent) claim 92, are in allowable condition and such action is respectfully requested.

By this Response, the Applicant respectfully submits that independent claim 1, and therefore, dependent claims 2 - 17, and 20 - 52, therefrom, that independent claim 53, and therefore, dependent claims 54 - 69, and 71 - 91 therefrom, and that independent claim 92, are in allowable condition and such action is respectfully requested.

An early Notice of Allowance is therefore respectfully requested.

Respectfully submitted,

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